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EXAMINER	
IQBAL, NADEEM	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 09/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,323	BIGBEE ET AL.	
	Examiner	Art Unit	
	Nadeem Iqbal	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-14,16-23 and 25-30* is/are rejected.

7)☐ Claim(s) *7,15 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *010202*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-6, 8-14, 16-23, 25-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blomgren (U.S. Patent number 5828578).

4. As per claim 1, Blomgren teaches (col. 2, lines 1-3) a dual processor die has a first CPU core and a second CPU core and a shared memory. He also teaches (col. 2, lines 8-10) that the first die is marked as defective when the shared memory is determined to contain an un-repairable defect. He also teaches to apply stimuli to determine if the first or the second CPU core is defective. He also teaches that the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is successively made. He thus teaches virtually ejecting a device from the data processing system in response to initiating the

platform-independent device removal sequence. He also teaches to service an event associated with the device in response to virtually ejecting the device from the data processing system, since he teaches as stated above to determine if the first or the second CPU core is defective, the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is successively made. He does not explicitly disclose to initiate a platform-independent device removal sequence for the device in response to detection of an event associated with the device. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to realize that He would initiate a device removal sequence as claimed, since He teaches to apply stimuli to determine if the first or the second CPU core is defective and that the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is successively made, therefore would inherently include to initiate a platform-independent device removal sequence for the device in response to detection of an event associated with the device.

5. As per claim 2, He does not explicitly disclose generating a system control interrupt responsive to detecting an event. He already teaches as stated per claim 1 above to determine if the first or the second CPU core is defective, the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is successively made. He therefore has to generate a system control interrupt to cause the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is successively made.

6. As per claim 3, Examiner takes official notice that it is well know in the art to utilize an INT_OUT command to generate a system control interrupt.

7. As per claim 4, He already teaches per claim 1 above that to apply stimuli to determine if the first or the second CPU core is defective. He also teaches that the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is successively made. He thus teaches to operate the first processor and the second processor in a functional redundancy check mode.

8. As per claim 5, He teaches per claim 1 above that to apply stimuli to determine if the first or the second CPU core is defective. He thus performs detecting an error as claimed.

9. As per claim 6, Examiner takes official notice that it is well know in the art to disable interrupts to a processor responsive to platform-independent device removal sequence, since none of the processor are available during testing and marking the other dual processor die, which is performed by Blomgren (col. 2, lines 20-22).

10. As per claim 8, Blomgren teaches (col. 5, lines 28-30) that the bonding option can disconnect cache memory from the defective CPU core, or by disconnecting its interconnect bus. He thus would disable the functional redundancy check mode responsive to detecting an error.

11. As per claim 9, He also teaches (col. 5, lines 30-33) that the bonding option may also disable a defective CPU core by preventing state machines in its control logic from leaving the reset state.

12. As per claim 10, He teaches as stated per claim 1 above to apply stimuli to determine if the first or the second CPU core is defective. He also teaches that the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is successively made. He thus teaches virtually inserting the device into the data processing system in response to initiating the platform-independent device removal sequence.

13. As per claim 11, Blomgren substantially teaches the claimed invention as disclosed related to claim 1 above. He also teaches (col. 2, lines 8-10) that the first die is marked as defective when the shared memory is determined to contain an un-repairable defect. He also teaches to apply stimuli to determine if the first or the second CPU core is defective. He also teaches that the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is successively made. He thus teaches virtually ejecting a device from the data processing system in response to initiating the platform-independent device removal sequence. He also teaches to service an event associated with the device in response to virtually ejecting the device from the data processing system, since he teaches as stated above to determine if the first or the second CPU core is defective, the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is successively made. He does not explicitly disclose to initiate a platform-independent device removal sequence for the device in response to detection of an event associated with the device. It would have been obvious to a person of ordinary skill in the art to realize that He would initiate a device removal sequence as claimed, since He teaches to apply stimuli to determine if the first or the second CPU core is defective and that the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is successively made, therefore would inherently include to initiate a platform-independent device removal sequence for the device in response to detection of an event associated with the device.

14. As per claim 12, He already teaches per claim 1 above that to apply stimuli to determine if the first or the second CPU core is defective. He also teaches that the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is

successively made. He thus teaches to operate the first processor and the second processor in a functional redundancy check mode.

15. As per claim 13, He teaches per claim 1 above that to apply stimuli to determine if the first or the second CPU core is defective. He thus performs detecting an error as claimed.

16. As per claim 14, Examiner takes official notice that it is well know in the art to disable interrupts to a processor responsive to platform-independent device removal sequence, since none of the processor are available during testing and marking the other dual processor die, which is performed by Blomgren (col. 2, lines 20-22).

17. As per claim 16, Blomgren teaches (col. 5, lines 28-30) that the bonding option can disconnect cache memory from the defective CPU core, or by disconnecting its interconnect bus. He thus would disable the functional redundancy check mode responsive to detecting an error.

18. As per claim 17, He also teaches (col. 5, lines 30-33) that the bonding option may also disable a defective CPU core by preventing state machines in its control logic from leaving the reset state.

19. As per claim 18, Blomgren teaches (col. 2, lines 1-3) a dual processor die has a first CPU core and a second CPU core and a shared memory. He also teaches (col. 2, lines 8-10) that the first die is marked as defective when the shared memory is determined to contain an un-repairable defect. He also teaches to apply stimuli to determine if the first or the second CPU core is defective. He also teaches that the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is successively made. He thus teaches virtually ejecting a device from the data processing system in response to initiating the platform-independent device removal sequence. He does not explicitly disclose to initiate a

platform-independent device removal sequence for the device in response to detection of an event associated with the device. It would have been obvious to a person of ordinary skill in the art to realize that He would initiate a device removal sequence as claimed, since He teaches to apply stimuli to determine if the first or the second CPU core is defective and that the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is successively made, therefore would inherently include to initiate a platform-independent device removal sequence for the device in response to detection of an event associated with the device.

20. As per claim 19, He does not explicitly disclose generating a system control interrupt responsive to detecting an event. He already teaches as stated per claim 1 above to determine if the first or the second CPU core is defective, the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is successively made. He therefore has to generate a system control interrupt to cause the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is successively made.

21. As per claim 20, Examiner takes official notice that it is well know in the art to utilize an INT_OUT command to generate a system control interrupt.

22. As per claim 21, He already teaches per claim 1 above that to apply stimuli to determine if the first or the second CPU core is defective. He also teaches that the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is successively made. He thus teaches to operate the first processor and the second processor in a functional redundancy check mode.

23. As per claim 22, He teaches per claim 1 above that to apply stimuli to determine if the first or the second CPU core is defective. He thus performs detecting an error as claimed.

24. As per claim 23, Examiner takes official notice that it is well know in the art to disable interrupts to a processor responsive to platform-independent device removal sequence, since none of the processor are available during testing and marking the other dual processor die, which is performed by Blomgren (col. 2, lines 20-22).

25. As per claim 25, Blomgren teaches (col. 5, lines 28-30) that the bonding option can disconnect cache memory from the defective CPU core, or by disconnecting its interconnect bus. He thus would disable the functional redundancy check mode responsive to detecting an error.

26. As per claim 26, He also teaches (col. 5, lines 30-33) that the bonding option may also disable a defective CPU core by preventing state machines in its control logic from leaving the reset state.

27. As per claim 27, He teaches as stated per claim 1 above to apply stimuli to determine if the first or the second CPU core is defective. He also teaches that the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is successively made. He thus teaches virtually inserting the device into the data processing system in response to initiating the platform-independent device removal sequence.

28. As per claim 28, Blomgren teaches (col. 2, lines 8-10) that the first die is marked as defective when the shared memory is determined to contain an un-repairable defect. He thus teaches a first firmware interface to detect an event associated with a processor within a data processing system. He also teaches to apply stimuli to determine if the first or the second CPU core is defective. He also teaches that the temporary electrical contacts with the first die is

removed and the electrical contacts with the other dual-processor is successively made. He thus teaches a second firmware interface to initiate a platform-independent device removal sequence for a processor in response to initiating the platform-independent device removal sequence. He does not explicitly disclose to initiate a platform-independent device removal sequence for the device in response to detection of an event associated with the device. It would have been obvious to a person of ordinary skill in the art to realize that He would initiate a device removal sequence as claimed, since He teaches to apply stimuli to determine if the first or the second CPU core is defective and that the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is successively made, therefore would inherently include to initiate a platform-independent device removal sequence for the device in response to detection of an event associated with the device.

29. As per claim 29, He does not explicitly disclose generating a system control interrupt responsive to detecting an event. He already teaches as stated per claim 1 above to determine if the first or the second CPU core is defective, the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is successively made. He therefore has to generate a system control interrupt to cause the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is successively made.

30. As per claim 30, He teaches as stated per claim 1 above to apply stimuli to determine if the first or the second CPU core is defective. He also teaches that the temporary electrical contacts with the first die is removed and the electrical contacts with the other dual-processor is

successively made. He thus teaches virtually inserting the device into the data processing system in response to initiating the platform-independent device removal sequence.

Allowable Subject Matter

31. Claims 7, 15 & 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nadeem Iqbal whose telephone number is (703)-308-5228. The examiner can normally be reached on M-F (8:00-5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703)-305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nadeem Iqbal
Primary Examiner
Art Unit 2114

NI